Franz Inc. Chief Scientist John Foderaro part of the UC-Berkeley RISC team receiving IEEE Milestone Recognition

Oakland, CA – February 2, 2015 – UC-Berkeley will receive IEEE Milestone recognition for their RISC Project on Feb 12, 2015. The UC-Berkeley RISC milestone plaque will be unveiled at 3:30 PM in the lobby on the 3rd floor of Soda Hall, Berkeley's Computer Science building. Speakers will include IEEE 2015 President Howard Michel, Professor David Patterson, and several others.

UC-Berkeley students designed and built the first VLSI reduced instruction-set computer in 1981. The simplified instructions of RISC-I reduced the hardware for instruction decode and control, which enabled a flat 32-bit address space, a large set of registers, and pipelined execution. A good match to C programs and the Unix operating system, RISC-I influenced instruction sets widely used today, including those for game consoles, smartphones and tablets.

In the 1970s, the general trend in in computer design was to increase the complexity of computer architectures. The thought was that this would best exploit the rapidly advancing capabilities of semiconductor technology. The popular DEC VAX 11-780 was the leading example. About 280 machine-language instructions were implemented in the VAX hardware. The VAX 11-780, a so-called super minicomputer, was advertised as exercising 1 million instructions/second and sold for about $100,000. This class of computers was then termed **CISCs, or** complex **instruction set computers.**

UC-Berkeley Professors David Patterson and Carlo Sequin

observed that compilers for high-level computer languages, such as C, rarely utilized the added instructions. They thought that overall performance could be improved by optimizing the combination of processor function and memory on a single chip. Better overall performance at a much lower cost might be achieved by simplifying the processor, thereby allowing more chip area to be devoted to memory. Thus the goal was defined as a RISC, **or reduced instruction set computer**.

The RISC-I project was initiated in 1980 with assignments in a sequence of graduate classes at UC-Berkeley, aiming to validate the RISC hypothesis. Initial conclusions based on simulation were positive, so the project continued, with critical grant support from DARPA. Students designed a processor with just 31 instructions, each executed in a single clock cycle. Included on the same student-designed chip, were 78 32-bit registers. This was enough memory to enable one-cycle execution of a large fraction of the instructions in compiled code.

Prior to receiving his Phd from UC-Berkeley, Foderaro worked on the design and testing of the Berkeley RISC-I processor. Part of the work was the low-level layout of some of the registers on the RiISC-I chip. His major contribution to the project was the design and development of a multi-level symbolic VLSI simulation language: Slang. Slang made use of Lisp’s unique ability to work at a symbolic or numeric level, and to interact closely with programs in other languages. Slang allowed users to design and simulate chip logic. It also could generate the Programmable Logic Array (PLA) description of the logic the user entered. A PLA is what is actually placed on the chip to drive the gates on the chip at the appropriate times. Once the chip was designed, a low-level circuit extractor and simulator read and ran the design and Slang worked with it to verify that the circuit layout was correct. Finally when the chips were manufactured, Slang controlled the chip tester by generating test vectors and

analyzing test results.

For additional information regarding this IEEE Milestone award, see here.

About John Foderaro

John Foderaro is the Chief Scientist and a Co-Founder of Franz Inc. Prior to Franz, John received a Ph.D. in Computer Science from the University of California, at Berkeley. While at UC Berkeley he wrote the original compiler for Berkeley's Lisp system, designed and implemented an entire new language for computer algebra, and worked on the "RISC" project which was later used as the blueprint for the SPARC processor out of Sun Microsystems. At Franz, Dr. Foderaro' work has been key in the development of Franz's industry leading graph database, AllegroGraph, which enables deployment of semantic graph applications. In addition to being the Chief Designer and implementer of Allegro Common Lisp and associated layered products, John designed and developed AllegroCache, a new OODB capable of handling billions of objects. It represents the next-generation object database technology.

About Franz Inc.

Franz Inc. is an innovative technology company with expert knowledge in developing and deploying graph search solutions. AllegroGraph, Franz's high-performance, transactional, and scalable graph database, provides the solid storage layer for powerful Enterprise grade NoSQL solutions. Franz's products and professional services are uniquely positioned to help bring your complex ideas to reality.